Claims:

1. A method for reducing the leakage current through a charge protection device in an integrated circuit, the method comprising:

reverse body biasing the charge protection device when the integrated circuit is in operation.

2. The method of claim 1, wherein reverse body biasing the charge protection device includes reverse body biasing the charge protection device when the integrated circuit is not experiencing an electro-static discharge event.

3. The method of claim 1, wherein the charge protection device comprises a transistor having a source region and a bulk region, and reverse body biasing the charge protection device includes applying a voltage potential to the bulk region of the transistor that is higher than a voltage potential of the source region.

4. The method of claim 1, further comprising removing a reverse body biasing voltage potential when the integrated circuit experiences an electro-static discharge event.

5. The method of claim 4, wherein the charge protection device comprises a transistor having a bulk region, and the method further comprising applying a power supply voltage potential to the bulk region of the transistor during an electro-static

discharge event.

6. An apparatus comprising:

an integrated circuit;

a charge protection device coupled to the integrated circuit; and

a resistive element adapted to reverse bias the charge protection device.

7. The apparatus of claim 6, wherein the charge protection device comprises a first transistor having a source region and a bulk region, the resistive element being coupled to the bulk region of the transistor.

8. The apparatus of claim 7, wherein the first transistor comprises a p-channel transistor.

9. The apparatus of claim 7, wherein the charge protection device comprises a second transistor coupled to the first transistor.

10. The apparatus of claim 9, wherein the first transistor and the second transistor are in series between the power supply voltage potentials.

11. The apparatus of claim 6, wherein the resistive element comprises an n-channel transistor.

12. The apparatus of claim 11, wherein the apparatus is adapted to apply a power supply voltage potential to the integrated circuit, and wherein the apparatus is further adapted to apply a voltage potential that is higher that the power supply voltage potential to a source region of the n-channel transistor.

13. The apparatus of claim 6, wherein the integrated circuit comprises a logic transistor having a gate oxide, and the resistive element comprises a transistor having a gate oxide that is thicker than the gate oxide of the logic transistor.

14. The apparatus of claim 7, wherein the first transistor has a width of at least 500 microns, a channel length of less than about 0.2 microns, and is adapted to conduct at least 1 pulsed amp.

15. An apparatus comprising:

an integrated circuit; and

a charge protection device coupled to the integrated circuit, the charge protection device comprising a first transistor and a second transistor, wherein the first transistor and the second transistor are arranged in series.

16. The apparatus of claim 15, further comprising a voltage divider adapted to apply a voltage potential to a gate terminal of the first transistor that is lower than a power supply voltage potential.

17. The apparatus of claim 16, further comprising a voltage buffer coupled to the gate terminal of the first transistor and the voltage divider.

18. An apparatus comprising:

a first transistor; and

a second transistor coupled to the first transistor, wherein the second transistor is reverse body biased when the first transistor is in operation, and is adapted to provide an impedance path during an electro-static discharge event that is lower than an impedance path provided by the first transistor.

19. The apparatus of claim 18, further comprising a resistive element coupled to the second transistor, the resistive element adapted to reverse bias the second transistor.

20. The apparatus of claim 19, wherein the resistive element is coupled to a voltage potential that is higher than a power supply voltage potential coupled to the first transistor.

21. The apparatus of claim 20, wherein the resistive element comprises a third transistor.

22. The apparatus of claim 19, wherein the resistive element comprises a third transistor that has a gate oxide that is thicker than a gate oxide of the first transistor.